



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,810	07/28/2003	Hung-Kun Chen	7256	4547

55740 7590 11/01/2006
GAUTHIER & CONNORS, LLP
225 FRANKLIN STREET
SUITE 2300
BOSTON, MA 02110

EXAMINER
LEE, SIU M

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/628,810

Applicant(s)

CHEN, HUNG-KUN

Examiner

Siu M. Lee

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 7/28/2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (indicated in page 3, lines 28-29). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2 and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhu et al. (US 2004/0005022 A1).

(1) Regarding claim 1:

Zhu et al. discloses a method of estimating frequency offset comprising the steps of:

receiving a sequence of signal samples (received signal samples r_m) which are complex numbers (as the conjugate of the samples r_m can be form later, it indicates that r_m is complex) (r_m in figure 7, paragraph 0102, line 2); and

delaying said signal samples by a first delay value (delay by (T_d) Buffer 1 in figure 7) (paragraph 0102, lines 3-5); and

performing multiplication between each said signal sample and a complex conjugate of each said delayed signal sample (the multiplier under buffer 1 in figure 7) (the product of a said sample and the conjugate of a said delayed sample, paragraph 0102, lines 3-5) to generate a first value (product from the multiplier in figure 7); and

delaying each said first value by a second delay value (delay by (T_w) Buffer 2 in figure 7) (paragraph 0102, lines 5-6); and

accumulating said first value to generate a second value (the adder under Buffer 2 in figure 7) (paragraph 0102, lines 6-7); and subtracting each said delayed first value from said second value to generate a third value ($P(d)$) (the output of the adder under Buffer 2 in figure 7) (paragraph 0102, lines 6-7); and

generating said estimated frequency offset based on said third value ($P(d)$ is used for frequency synchronization, paragraph 0103, lines 1-2, paragraph 0129, lines 4-9 and paragraph 0130).

(2) Regarding claim 2:

Zhu et al. discloses that second delay value is larger than said first delay value ($T_d = T_{\text{short}}$ and $T_w = 7T_{\text{short}}$, paragraph 0142, lines 6-8).

(3) Regarding claim 8:

Zhu et al. discloses a receiver receiving an analog signal, said device comprising:

an analog-to-digital converter for converting said received analog signal to a sequence of sampled elements (analog-to-digital converter 22 and 23 in figure 4, paragraph 0074, lines 17-18);

a first storing means (Buffer 1 in figure 7) having M elements (D samples) (paragraph 0102, lines 2-3) that sequentially stores said sampled elements, for delaying each said sampled elements by M samples (D samples) to generate a delayed sampled element;

a multiplication means (the multiplier under Buffer 1 in figure 7) for performing multiplication between a complex conjugate of said delayed sampled element and a current sampled element (paragraph 0102, lines 3-5);

a second storing means (Buffer 2 in figure 7) having N elements (W samples) that sequentially stores an output of said multiplication means, for delaying each said output of said multiplication means by N samples (paragraph 0102, lines 5-6);

an accumulating means (the adder under Buffer 2 in figure 7) for accumulating said output of said multiplication means; and

a subtracting means (the adder under Buffer 2 in figure 7) for sequentially subtracting output of said second storing means from output of said accumulating means (T_d) (paragraph 0102, lines 6-7);

an estimating means (2-stage estimation method in figure 14, paragraph 0142, lines 1-3) for generating said estimated frequency offset based on an output of said subtracting means (the phase shift can be estimated by calculating the argument of $P(d)$, paragraph 0129, lines 9-14 and paragraph 0130).

(4) Regarding claim 9:

Zhu et al. discloses a device of claim 8, wherein the value of N (W) is larger than the value of $M(D)$ ($T_d = T_{\text{short}}$ and $T_w = 7T_{\text{short}}$, paragraph 0142, lines 6-8).

3. Claims 3-4, 7, 10-12, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Scarpa (US 2004/0001563 A1).

(1) Regarding claim 3:

Scarpa discloses a method of estimating frequency offset in a receiver, comprising the steps of:

receiving a first portion of signal samples which are complex numbers (course frequency error estimate generated from a first portion of an OFDM preamble, since the conjugate of the preamble is created in 330 in figure 4, the preamble signal is a complex number) (paragraph 18, lines 4-6);

receiving a first control signal (control input L1 to the averager 336 in figure 4) (paragraph 0052, lines 1-3);

deriving a first frequency offset estimation (course estimate output from course frequency estimation module 336 in figure 4) based on said first portion of signal samples (paragraph 55, lines 1-3);

receiving a second portion of signal samples which follows said first portion of signal samples (second portion of the preamble) (paragraph 0061, lines 1-2);

compensating said second portion of signal samples by utilizing said first frequency offset estimation so as to generate a compensated second portion of signal samples (mixer 310 in figure 4 mixes the data input signal with the complex correction signal to generate the frequency corrected data signal) (paragraph 0048, lines 14-17);

deriving a second frequency offset estimation based on said compensated second portion of signal samples (fine est. in figure 4 output from the fine frequency estimation module 316 in figure 4) (paragraph 62, lines 10-16); and

obtaining a total frequency offset estimation based on said first frequency offset estimation and said second frequency offset estimation (the total frequency offset estimation is decide by the carrier frequency correction selection module 308 which includes a PPL 353 based on the coarse and fine frequency estimation in figure 4) (paragraph 0048, lines 1-9).

(2) Regarding claim 4:

Scarpa discloses a method wherein the first frequency offset estimation (coarse frequency estimate) keeps constant after the first control signal is active (paragraph 52, lines 5-8).

(3) Regarding claim 7:

Scarpa discloses a method wherein the step of deriving a second frequency offset estimation (long correction module) comprising the steps of:

delaying each of said partial compensated second portion of signal samples by a third delay value (delay Z^{-64} block 342 in figure 4) (paragraph 61, lines 8-9);

performing multiplication (mixer 340 in figure 4) between each said partial compensated signal sample and a complex conjugate (conj 344 in figure 4) of each said delayed partial compensated signal sample to generate a fourth value (paragraph 61, lines 3-9);

accumulating said fourth value to generate a fifth value (summation module 346 in figure 4) (paragraph 61, lines 3-9);

generating said second frequency offset estimation based on said fifth value (fine frequency offset generate by fine frequency module 316 in figure 4).

(4) Regarding claim 10:

Scarpa discloses a device of estimating frequency offset in a receiver comprising:

first deriving means (short correlation module 302 and coarse frequency estimation module 306 in figure 4) for deriving a first frequency offset estimation based on a first portion of said signal samples (paragraph 18, lines 4-6);

compensating means (complex mixer 310 in figure 4) for compensating a frequency offset of a second portion of said signal samples which follows said first portion of signal samples by utilizing said first frequency offset estimation so as to generate a compensated second portion of signal samples (paragraph 0048, lines 14-17);

second deriving means (long correlation module 312 and fine frequency estimation module 316 in figure 4) for deriving a second frequency offset estimation based on said compensated second portion of signal samples (paragraph 62, lines 10-16);

estimating means (carrier frequency correction selection module 308 in figure 4) for computing a total frequency offset estimation based on said first frequency offset estimation and said second frequency offset estimation (paragraph 0048, lines 1-9).

(5) Regarding claim 11:

Scarpa discloses a device of estimating frequency offset in a receiver wherein the device further receives a first control signal (control signal L1 to the averager 336 in figure 4), and said first frequency offset estimation keeps constant after said first control signal is active (paragraph 52, lines 5-8).

(6) Regarding claim 12:

Scarpa discloses a device of estimating frequency offset in a receiver wherein the device further receives a second control signal (control signal L2 to the averager 348 in figure 4), and said first frequency offset estimation keeps constant after said first control signal is active (paragraph 0062, lines 10-11).

(7) Regarding claim 15:

Scarpa discloses a method wherein said deriving means for deriving a second frequency offset estimation comprising:

a delaying unit (delay Z^{-64} block 342 in figure 4) for delaying each of said partial compensated second portion of signal samples (paragraph 61, lines 8-9);

a multiplication unit (mixer 340 I figure 4) for performing multiplication between each said partial compensated signal sample and a complex conjugate (conj 344 in figure 4) of each said delayed partial compensated signal sample to generate a fourth value (paragraph 61, lines 3-9);

an accumulating unit (summation module 346 in figure 4) for accumulating said fourth value to generate a fifth value (paragraph 61, lines 3-9); and

an estimating unit (fine frequency estimation module 316 in figure 4) for computing said second frequency offset estimation based on said fifth value.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5-6 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. (US 2004/0005022 A1) in view of Scarpa (US 2004/0001563 A1).

(1) Regarding claim 5:

Scarpa discloses all the subject matter as discussed in claim 3 except the step of deriving said first frequency offset estimation comprises the steps of delaying said first portion of signal samples by a first delay value; and performing multiplication between each said signal sample and a complex conjugate of each said delayed signal sample to generate a first value; and delaying each said first value by a second delay value; and accumulating said first value to generate a second value; and subtracting each said delayed first value from said second value to generate a third value; and generating said estimated frequency offset based in said third value.

Zhu et al discloses a receiver and method for WLAN for deriving a first frequency offset estimation comprises the steps of delaying said first portion of signal samples (delay by the Buffer 1 in figure 7) by a first delay value (T_d); and performing multiplication (the multiplier under buffer 1 in figure 7) between each said signal sample and a complex conjugate of each said delayed signal sample to generate a first value (the product of a said sample and the conjugate of a said delayed sample, paragraph 0102, lines 3-5) to generate a first value (product from the multiplier in figure 7); and delaying each said first value by a second delay value (delay by the Buffer 2 in figure 7); and accumulating said first value (the adder under Buffer 2 in figure 7) to generate a second value; and subtracting each said delayed first value from said second value to generate a third value (paragraph 0102, lines 6-7); and subtracting each said delayed first value from said second value to generate a third value ($P(d)$) (the output of the adder under Buffer 2 in figure 7) (paragraph 0102, lines 6-7); and generating said estimated frequency offset based in said third value ($P(d)$) is used for frequency

synchronization, paragraph 0103, lines 1-2, paragraph 0126, lines 4-9 and paragraph 0130).

It is desirable to derive a first frequency offset estimation as taught by Zhu et al. because it gives a precise detection of the symbol timing (paragraph 41, lines 3-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the method of deriving the first frequency offset in the system of Scarpa to improve the accuracy of the frequency offset estimation.

(2) Regarding claim 6:

Zhu et al. further discloses that said second delay value is larger than said first delay ($T_d = T_{\text{short}}$ and $T_w = 7T_{\text{short}}$, paragraph 0142, lines 6-8).

(3) Regarding claim 13:

Zhu et al. discloses a device wherein said first deriving means for deriving a first frequency offset estimation comprising:

a first delaying unit (Buffer 1 in figure 7) having M elements (D samples) for delaying each of said first portion of signal samples by M samples (D samples) to generate a delayed signal sample (paragraph 0102, lines 2-3);

a multiplication unit (the multiplier under Buffer 1 in figure 7) for performing multiplication between each said signal sample and a complex conjugate of each said delayed signal sample to generate a first value (paragraph 0102, lines 3-5);

a second delaying unit (Buffer 2 in figure 7) having N elements (W samples) for delaying each said first value by N samples to generate a delayed first value (paragraph 0102, lines 5-6);

an accumulating unit (adder under Buffer 2 in figure 7) for accumulating said first value to generate a second value (paragraph 0102, lines 6-7);

a subtracting unit (the adder under Buffer 2 in figure 7 with the minus sign) for sequentially subtracting each said delayed first value from said second value to generate a third value (paragraph 0102, lines 6-7); and

an estimating unit (2 stage estimation method in figure 14, paragraph 0142, lines 1-3) for computing said first frequency offset estimation based on said third value (the phase shift can be estimated by calculating the argument of $P(d)$, paragraph 0129, lines 9-14 and paragraph 0130).

It is desirable to derive a first frequency offset estimation as taught by Zhu et al. because it gives a precise detection of the symbol timing (paragraph 41, lines 3-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the method of deriving the first frequency offset in the system of Scarpa to improve the accuracy of the frequency offset estimation

(4) Regarding claim 14:

Scarpa further discloses wherein the value of N is larger than the value of M ($T_d = T_{\text{short}}$ and $T_w = 7T_{\text{short}}$, paragraph 0142, lines 6-8).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kim (US 7,058,151 B1) discloses an apparatus and method for achieving symbol timing and frequency synchronization to orthogonal frequency division

multiplexing signal. You et al. (US 2003/0112743 A1) discloses a timing synchronization for OFDM-based wireless networks. Moose (US 2002/0065047 A1) discloses a synchronization, channel estimation and pilot tone tracking system. Vanderperren et al (US 2004/0076246 A1) discloses a methods and apparatus for synchronization of training sequences.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 10/628,810
Art Unit: 2611

Page 14

Siu M. Lee
10/25/2006

A handwritten signature in black ink, appearing to read "Chieh M. Fan", with a stylized flourish at the end.

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER